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*Research Article*

# The Cascade Carry Array Multiplier – A Novel Structure of Digital Unsigned Multipliers for Low-Power Consumption and Ultra-Fast Applications

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**Abstract: This article presents a low power consumption, high speed multiplier, based on a lowest transistor count novel structure when compared with other traditional multipliers. The proposed structure utilizes 4×4-bit adder units, since it is the base structure of digital multipliers. The main merits of this multiplier design are that: it has the least adder unit count; ultra-low power consumption and the fastest propagation delay in comparison with other gate implementations. The figures demonstrate that the proposed structure consumes 32% less power than using the bypassing Ripple Carry Array (RCA) implementation. Moreover, its propagation delay and adder units count are respectively about 31% and 8.5% lower than the implementation using the bypassing RCA multiplier. All of these simulations were carried out using the HSPICE circuit simulation software in 0.18 μm technology at 1.8 V supply voltage. The proposed design is thus highly suitable in low power drain and high-speed arithmetic electronic circuit applications.**

**Keywords:** ***Cascade Carry Array Multiplier; Propagation Delay; Ripple Carry Array Multiplier (RCA); Braun Multiplier; Bypassing RCA; Bypassing CSA; Carry Save Array; Ripple Carry Array.***

## 1. Introduction

With the exponential growth in the number of laptops, portable personal communication systems and the continuation of shrinking chip fabrication technology, research effort in creating even low-power microelectronic devices has been intensified. Today, there are an increasing number

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of portable applications requiring an ever smaller and smaller die (chip) area, even lower power consumption with the highest throughput possible. Therefore, circuits with the lowest power consumption become the major candidate for the design of microprocessor and system components [1-4]. While the growth of the electronics market has driven the Very Large-Scale Integration (VLSI) industry towards Ultra Large-Scale Integration (ULSI), ultra-high integration density and System-on-Chip (SoC) designs and beyond few GHz clock cycle operating frequencies - critical concerns have been arising regarding the severe escalation in power consumption and the need to drastically reduce it [5], including the consequent heat generation and how to dissipate it.

Multiplication is one of the most important and fundamental operations in digital computer systems and in digital signal processors or DSP chips. However, multipliers are very power-hungry components, so reducing their power consumption is a key to satisfying the overall power budget of digital VLSI/ULSI circuits. Various techniques can be applied externally or with internal techniques that deal with the input data characteristics. These internal techniques are concerned with modifying the architecture, logic and circuit designs of the traditional multiplier circuit [5]. The primary concern of electronic portable devices is to extend their operating hours without changing the battery residing in the device. Although advanced power saving technology and energy management software have enhanced and prolonged the battery life to operate for longer hours, the complicated and intensive operations in high-end portable devices are still power hungry and it is thus critical to implement the low power design [6] immediately.

For designing multipliers to achieve this goal, currently two solutions exist. The first option is by altering the design of the overall structure; the second way is by internally redesigning the adder units that constitute the multiplier itself. In electronic device applications, multipliers perform all of the operations and are thus required to have the discussed desirable characteristics of: efficient utilization of power, low propagation delay, high throughput, lowest energy per instruction (EPI) consumption and low latency [7], [8]. In recent years, many small-sized multiplier circuits have been proposed that offer lower propagation delay, low-power dissipation and low-power rating of input bits [7-9]. Since power consumption determines the time between two successive recharges of such a device, as well as the device's battery life, the reduction of power dissipation is vital in such devices. The main source of power dissipation in a complementary pass transistor logic circuit is the switching activity of its nodes, which may contribute to more than 90% of the total power consumption [8], [10], and [11]. The five important parameters for VLSI design are the: power requirement, delay between the input and the output, chip or die area, power delay product (PDP) and energy delay product (EDP) - with the EDP being the most important parameter for optimization in VLSI circuits [12-13]. Each proposed structure of the multiplier or adder unit has its own advantages and disadvantages.

The total power dissipated in a generic digital complementary metal–oxide–semiconductor (CMOS) gate is calculated as shown by Equations (1)-(4):

$$P_{Total} = P_{Dynamic} + P_{Short\ Circuit} + P_{Static} \quad (1)$$

$$P_{Dynamic} = P \,.\, C_L \,.\, f \,.\, V^2_{DD} \quad (2)$$

$$P_{Short\ Circuit} = I_{peak} \,.\, t_{SC} \,.\, V_{DD} \,.\, f \quad (3)$$

$$P_{Static} = I_{Static} \,.\, V_{DD} \quad (4)$$

In the above equations $P$, $f$, $C_L$, $V_{DD}$, $I_{peak}$, $t_{SC}$ and $I_{Static}$ are, respectively, change state probability of gate, simulation frequency, capacitor of gate, supply voltage, maximum current during changing the status of gate, short circuit time and static current. The static power that is shown in Eq. (4), is very important in circuits operating under a low supply voltage [12-14].

There is considerable delay between receiving the inputs and delivering the outputs, since several adder units exist along this path. Moreover, another harmful effect impacts on our data, which is called the glitch effect and it causes a significant increase in the power consumption. To overcome these problems, researchers are compelled to reduce the gate count in these adder units as much as possible. The proposed design shows the implementation of a 4×4 bit multiplier circuit with the minimum adder unit count amongst the other multipliers which have been introduced up till now.

In this present paper, a new structure of the multiplier is proposed in order to implement the novel 4×4-bit multiplier circuit. The proposed structure is designed with the minimum number of adder unit count, so that it will have the lowest: power consumption, delay, PDP, EDP and die area. This article also describes the design of a new structure for the multipliers in digital applications, such as those used in digital signal processing (DSP) and for cryptographic and crypto-currency generation and blockchain algorithms. The proposed multiplier structure was simulated and the results compared with other structures of multipliers such as the Ripple Carry Array (RCA), array multiplier, Braun multiplier and bypassing multiplier based on carry-save array (CSA) and RCA. To simulate all of these structures the 28 transistor (28T) full adder cell was used to implement them all. Based on the simulation results, the proposed structure of the multiplier is the best present incarnation of the multiplier as far as is known.

The remainder of the paper is organized as follows: the 28T full adder cell is described in Section II; the illustration of the multiplier architectures are shown in Section III; Section IV is about the proposed multiplier based on a new "Cascade Carry Array" (CCA) multiplier; the simulation results of the proposed multiplier structure and its performance comparisons with the other multipliers are shown in Section V; finally, the conclusion is given in Section VI.

## 2. Conventional CMOS 28 Transistor (28T) Full Adder

The 28-transistor full adder is the pioneer of the CMOS (Complementary Metal Oxide Silicon Chip) traditional adder circuit. The schematic of this adder is shown in Figure 1, below. This adder cell is built using an equal number of N-type metal-oxide-semiconductor (NMOS) and P-type metal-oxide-semiconductor (PMOS) transistors. The main advantage this adder has is its complete output swing.

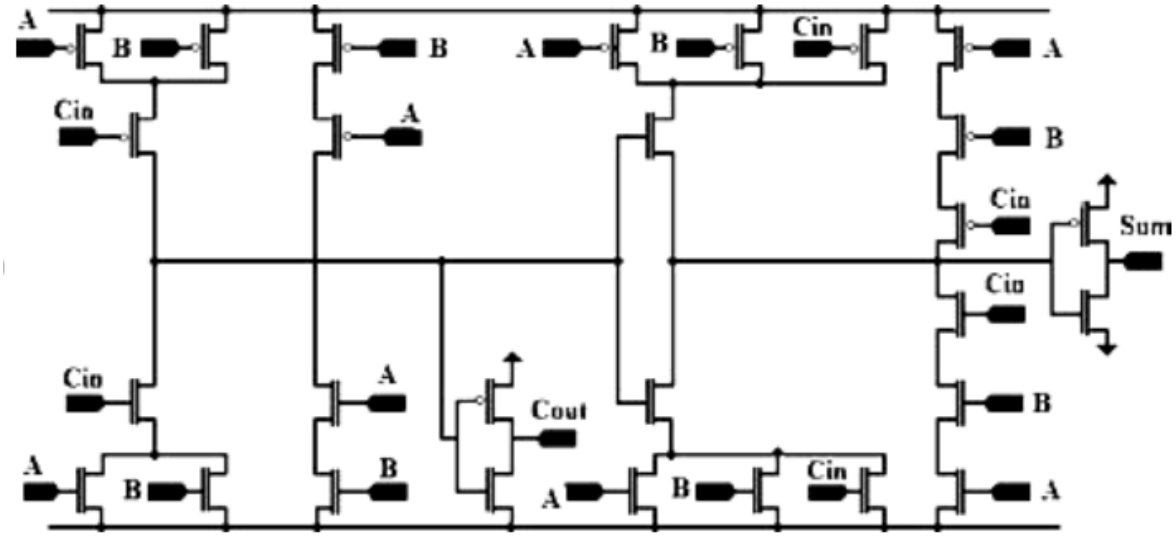


**Figure 1.** The Conventional 28 Transistor CMOS Adder. Reprinted with permission from [15].

## 3. Multiplier Architectures

Multipliers are in fact complex adder arrays. This is a common operation in a large number of applications. The complexity of this function has led to a large amount of research directed at speeding up its execution. A multiplier can be implemented using different algorithms. Some of the common structures of multipliers are shown in Figures 2-6. Since multiplication is the vital function in DSP processors and moreover, there exist a great deal of applications today requiring these processors as the core of their systems, optimizing them will surely speed-up the overall performance of these systems. The main objectives in this area are as follows:

- Increasing the processing speed by reducing the delay;
- Decreasing the propagation delay time as the most important factor amongst the other types of delay by using the least number of adder units;

- Mitigating power consumption by attenuating the effect of the glitch and
- Achieving more circuit integrity by using the least number of adder units as possible.

The aim of this study was to introduce a new CMOS multiplier structure to meet the above four goals.

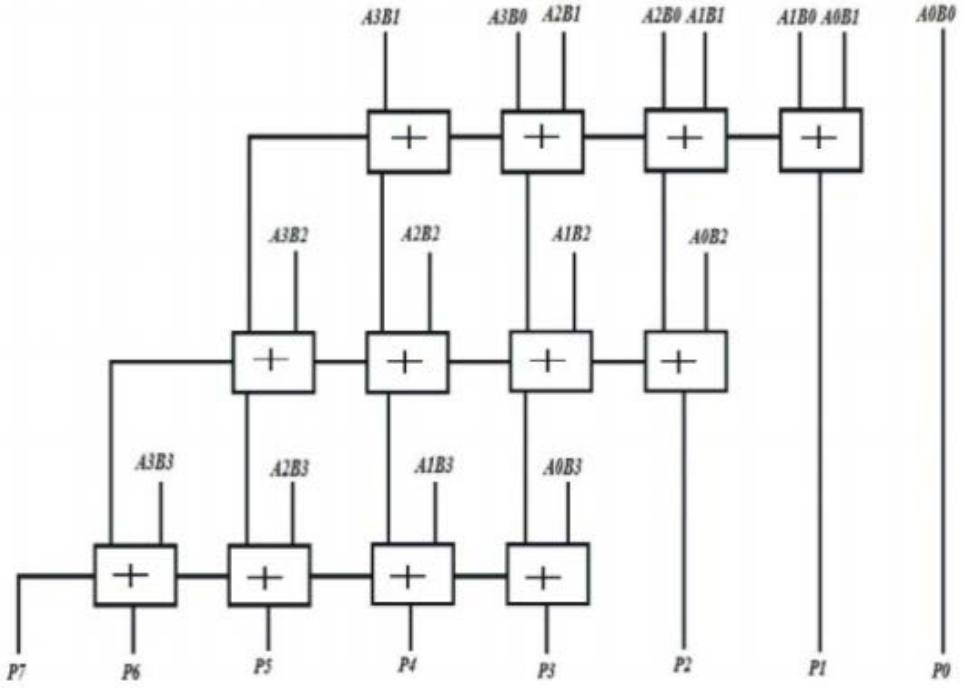


**Figure 2.** A 4×4 bit array multiplier [12], [16].

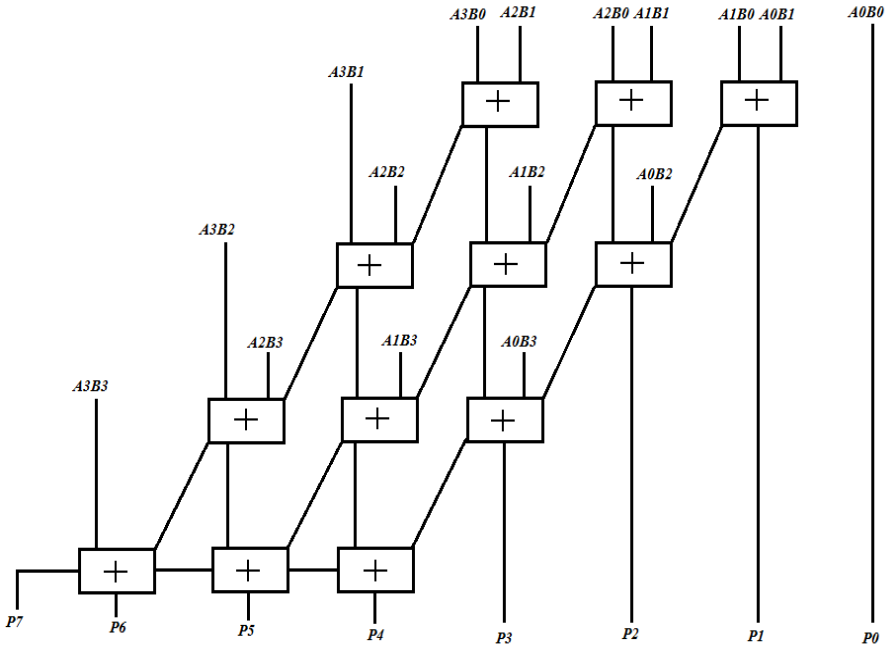


**Figure 3.** A 4×4 bit basic Braun multiplier [12], [16].

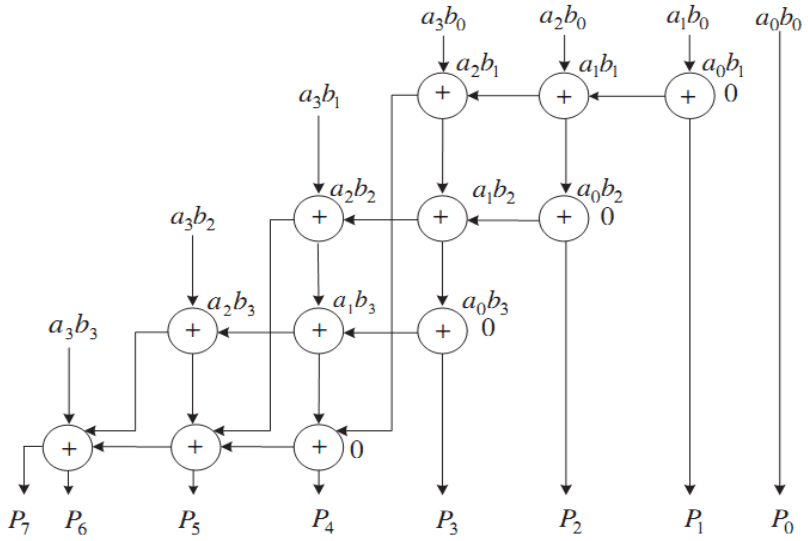


**Figure 4.** A 4×4 bit ripple carry array multiplier (RCA) [12], [16].

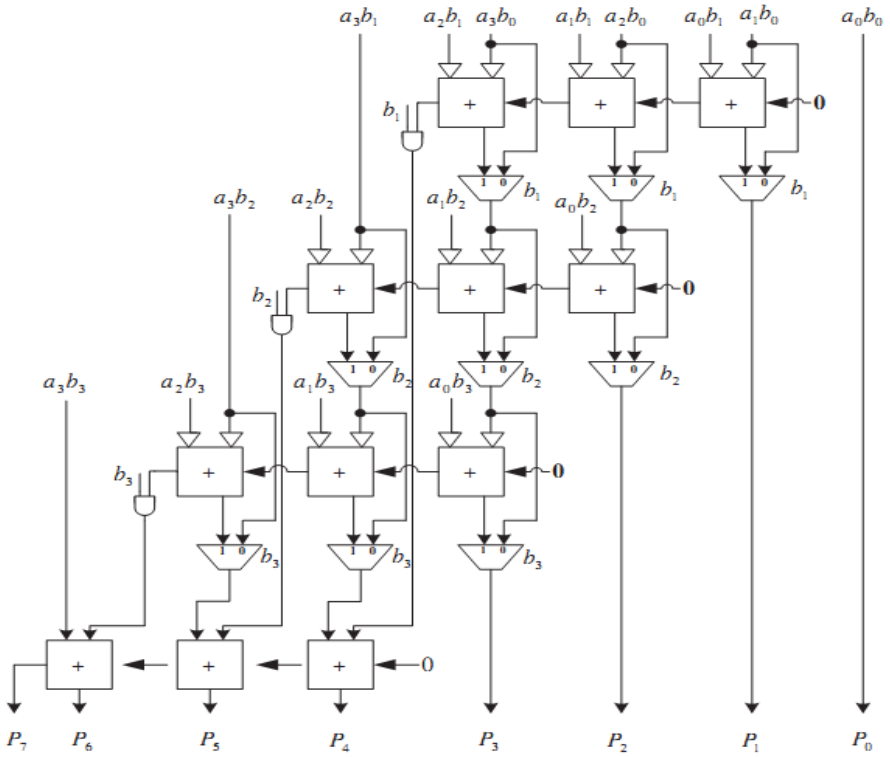


**Figure 5.** A 4×4 bit row bypassing multiplier based on RCA [12], [16].

## 4. Proposed Multiplier Based on a New Structure (CCA Multiplier)

This section presents the novel structure of the cascade carry array (CCA) multiplier design. This structure uses the minimum number of adder units, thus it has the fewest transistor count compared with the other structures. The CCA multiplier as designed also has the lowest propagation delay and power consumption, so consequently it also achieves a very low PDP and EDP as well. The proposed design is illustrated in Figure 7.

The following steps were taken to design the CCA multiplier. First of all, it was necessary to find a logical relation between the input and output bits. Then, it was important to attain a structure possessing the least high swing and ultra-low delay adder units along the path from the input to output which meets the requirements.

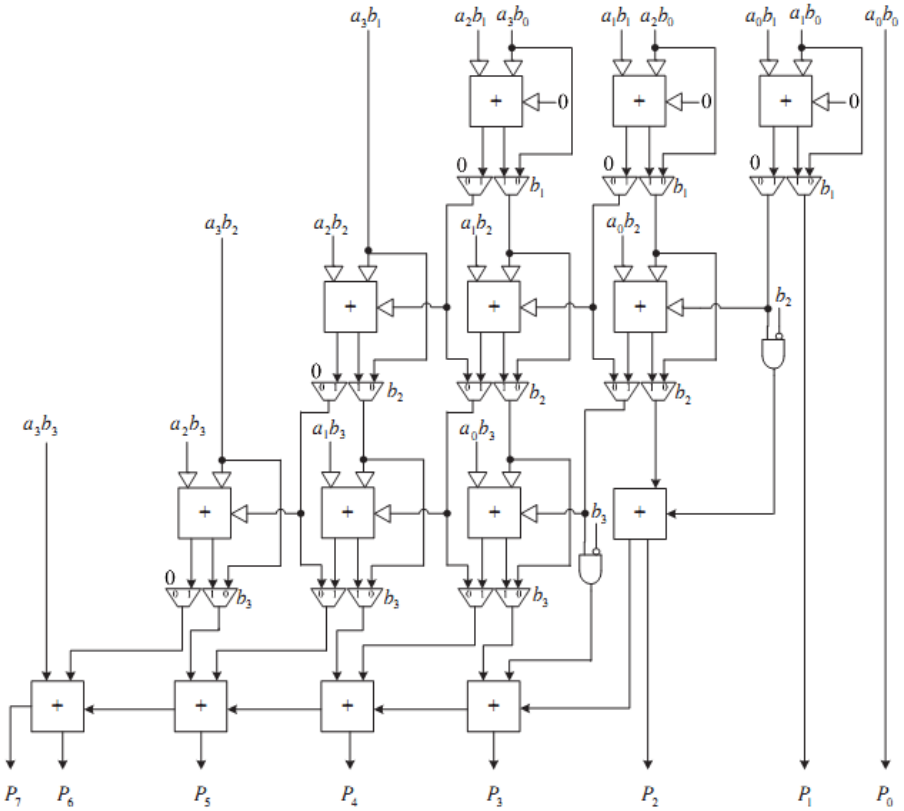


**Figure 6.** A 4×4 bit bypassing multiplier based on CSA [12], [16].

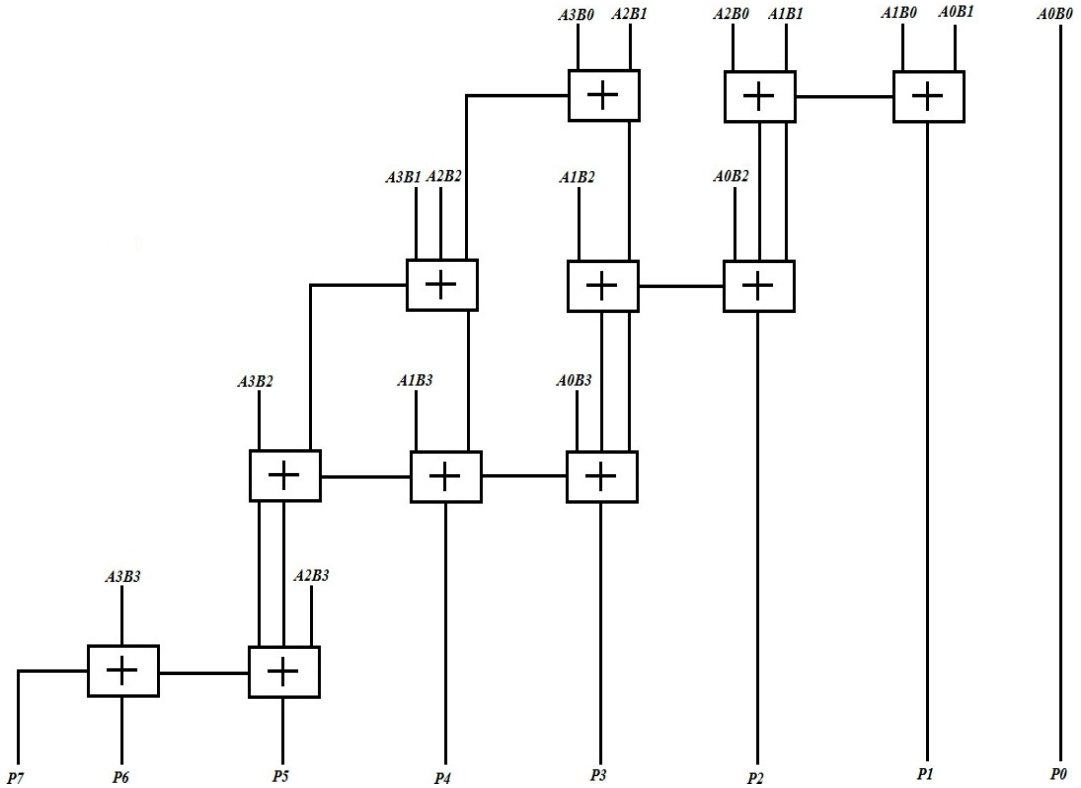


**Figure 7.** A 4×4 bit cascade carry array multiplier (CCA).

To choose the best full adder block in term of the delay and swing properties, prior structures were compared and the 28T full adder which met the goals better than the other structures was selected. After doing these steps, the novel proposed multiplier structure was simulated using the

industrial circuit simulation HSPICE (Simulation Program with Integrated Circuit Emphasis) software in order to investigate the obtained results and diagnose any of the probable malfunctions encountered.

In the final step, the proposed circuit was evaluated and compared with the other ones. Comparisons were done for the major characteristics, which were the average power, delay, PDP, EDP, and transistor count. All the multipliers were simulated using the 28T full adder cell library in 0.18 μm CMOS technology operating at a clock frequency of 100 MHz at an operating temperature of 27℃. The supply voltage was set to 1.8 V.

## 5. Simulations and Results

The HSPICE industrial circuit simulation software was used to carry out all these simulations. The proposed circuit was evaluated and compared with the other ones. All the multipliers were simulated by using the 28T full adder cell implemented using the 0.18μm CMOS technology files with a clock frequency of 100 MHz and at an operating temperature of 27°C with a supply voltage of 1.8 V. The simulation results of the different multipliers and the proposed CCA multiplier are given in Table 1. It is anticipated from the results that the CCA multiplier consumes the least power compared to the others. Moreover, the CCA multiplier has the lowest propagation delay, power delay product, energy delay product and die occupied area than the other structures.

**Table 1.** Result for 0.18 μm technology multiplier at 1.8 V supply voltage, 100 MHz clock frequency.

| Multiplier Design | Avg power (μW) | Delay (PS) | PDP (FJ) | EDP ($\times 10^{-25}$) | No. of Transistors |
|---|---|---|---|---|---|
| **Array** | 126.66 | 517.5 | 65.54 | 339.2 | 464 |
| **Braun** | 125.76 | 526.5 | 66.21 | 348.6 | 464 |
| **RCA** | 126.60 | 521.5 | 66.02 | 344.3 | 464 |
| **Bypassing RCA** | 164.84 | 509 | 83.90 | 427.0 | 655 |
| **Bypassing CSA** | 202.30 | 505.5 | 102.26 | 516.9 | 810 |
| **Proposed CCA** | 112.24 | 351.5 | 39.45 | 138.6 | 436 |

This is quite understandable as the proposed multiplier has a much lower transistor count, thus much lower internal capacitance than the others. Table 2, below, gives the percentage improvement of the proposed CCA multiplier over the other multiplier designs. Thus, the ranking of those multipliers in terms of power savings will be as follows: CCA Multiplier is the first, Braun Multiplier the second, RCA Multiplier the third, Array Multiplier the fourth, Bypassing RCA Multiplier the fifth, and Bypassing CSA Multiplier the sixth. The CCA multiplier speed improvements are also shown in Table 2. The percentage power-delay product reduction of the CCA multiplier (Fig. 7) over the other multipliers is shown on the fourth column of Table 2. Finally, the last column shows the savings in the number of transistors by using the proposed CCA multiplier.

**Table 2.** Results for the proposed CCA advantages over the other multiplier designs.

| Multiplier Design | CCA Power Saving (%) | CCA Speed Improvement (%) | CCA PDP Reduction (%) | CCA no. of Transistor Saving |
|---|---|---|---|---|
| **Array** | 11.38 | 32 | 39.8 | -28 |
| **Braun** | 10.75 | 32.23 | 40.41 | -28 |
| **RCA** | 11.34 | 32.59 | 40.24 | -28 |
| **Bypassing RCA** | 31.9 | 30.94 | 52.97 | -19 |
| **Bypassing CSA** | 44.51 | 30.46 | 61.42 | -374 |

## 6. Conclusions

This research has presented a high performance and low power CMOS array multiplier. There exist some major limitations in designing efficient multipliers such as gaining the desired delay and swing. A high delay leads to an increase in the glitch effect which increases the static power consumption that takes us away from realizing the high efficiency multiplier. Additionally, having a low output swing causes two main problems. Firstly, it may lead to wrong outputs and the other problem appears when it exceeds the regular power consumption level. The proposed multiplier overcomes these limitations by decreasing the power consumption and the propagation delay by removing the number of extra adder units needed to design the multiplier. This work primarily focused on designing the multiplier using the actual minimum number of adder units producing the least possible propagation delay. Intensive HSPICE simulation proved that the new structure possessed the lowest: power consumption, propagation delay, PDP and EDP. These results were obtained under HSPICE simulation at room temperature and using a power supply voltage of 1.8 V. With this proposed model, a multiplier possessing superlative features were obtained.

Future work will consist of designing a multiplier with carry bit prediction in order to lower the delay factor further.

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